

UNITED STATES PATENT APPLICATION FOR:

**NITROGEN-FREE DIELECTRIC
ANTI-REFLECTIVE COATING AND HARDMASK**


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NITROGEN-FREE DIELECTRIC ANTI-REFLECTIVE COATING AND HARDMASK

[0001] This application claims priority to United States Provisional Application No. 60/433,445, filed December 13, 2002 and United States Provisional Application No. _____ filed December 1, 2003 titled "Nitrogen-Free Dielectric Antireflective Coating and Hardmask," and is a continuation in part of United States Patent Application No 10/193,489 filed July 11, 2002.

BACKGROUND OF THE DISCLOSURE

Field of the Invention

[0002] The invention relates to the fabrication of integrated circuits and to a process for depositing dielectric layers on a substrate and the structures formed by the dielectric layers.

Description of the Related Art

[0003] One of the primary steps in the fabrication of modern semiconductor devices is the formation of metal and dielectric layers on a substrate by chemical reaction of gases. Such deposition processes are referred to as chemical vapor deposition or CVD. Conventional CVD processes supply reactive gases to the substrate surface where heat-induced or energy-enhanced chemical reactions take place to produce a desired layer.

[0004] Semiconductor device geometries have dramatically decreased in size since the devices were first introduced several decades ago. Since then, the number of devices that will fit on a chip doubles every two years. Tomorrow's plants soon will be producing devices with smaller geometries.

[0005] To further reduce the size of devices on integrated circuits, the industry is using conductive materials having low resistivity and insulators having low dielectric constants (dielectric constants of less than 4.0) to reduce the capacitive coupling between adjacent metal lines. One such low dielectric constant (low k) material comprises silicon, oxygen, and carbon and may be deposited as a dielectric material

in fabricating damascene features. One conductive material having a low resistivity is copper and its alloys, which have become the material of choice for sub-quarter-micron interconnect technology because copper has a lower resistivity than aluminum, ($1.7 \mu\Omega\text{-cm}$ compared to $3.1 \mu\Omega\text{-cm}$ for aluminum), a higher current and higher carrying capacity. These characteristics are important for supporting the higher current densities experienced at high levels of integration and increased device speed. Further, copper has desirable thermal conductivity and is available in a highly pure state.

[0006] Unfortunately, copper is difficult to etch and achieve a precise pattern. Etching with copper using traditional deposition and etch processes for forming interconnects has been less than satisfactory. Thus, new methods for manufacturing interconnects containing copper and low k dielectric materials are being developed.

[0007] One method for forming vertical and horizontal interconnects is by using damascene or dual damascene method. In the damascene method, one or more dielectric materials, including low k dielectric materials, are deposited and pattern etched to form the vertical interconnects (vias) and horizontal interconnects (lines). Conductive materials such as copper and barrier layer materials used to prevent diffusion of copper into the surrounding low k dielectric are then inlaid into the etched pattern. Any excess copper and barrier layer materials external to the etched pattern remaining on the field of the substrate are then removed.

[0008] However, low k dielectric materials are often porous and susceptible to interlayer diffusion of conductive materials which can result in the formation of short-circuits and device failure. A dielectric barrier layer material is used in copper damascene structures to reduce or to prevent interlayer diffusion. Traditional dielectric barrier layer materials often have high dielectric constants of 7 or greater. The combination of a high k dielectric material with surrounding low k dielectric materials results in dielectric stacks having a higher than desired dielectric constant.

[0009] Additionally, forming damascene structures requires the use of lithographic processes. For example, in process sequences using conventional

lithographic techniques, a layer of energy sensitive resist is formed over a stack of material layers on a substrate. Many of the underlying material layers are reflective to ultraviolet light. These reflections can distort the dimensions of features such as lines and vias that are formed in the energy sensitive resist material. This is troublesome when using 193 nm radiation with reflective metal layers. One technique proposed to minimize reflections from an underlying material layer uses an anti-reflective coating (ARC). The ARC is formed over the reflective material layer prior to resist patterning. The ARC suppresses the reflections of the underlying material layer during resist imaging, providing accurate pattern replication in the layer of energy sensitive resist.

[0010] However, conventional ARC materials contain nitrogen, including silicon nitride and titanium nitride. Nitrogen in the ARC layer may chemically alter the composition of the photoresist material. The chemical reaction between nitrogen and the photoresist material is referred to as photoresist poisoning. The altered photoresist material may not be lithographically patterned as expected and result in imprecisely formed features in the photoresist material or excessive photoresist residue remaining on the substrate surface after photoresist patterning, both of which can detrimentally affect subsequent processes, such as etching processes. For example, nitrogen may neutralize acid near a photoresist and ARC interface and result in residue formation, known as footing, which can further result in curved or rounded aspects at the interface of the bottoms and sidewalls of features rather than desired right angles.

[0011] Additionally, low k materials are susceptible to surface defects or feature deformation during polishing and removal of conductive materials under conventional polishing processes. One solution to limit or reduce surface defects and deformation is to deposit a hardmask over the exposed low k materials prior to patterning and etching feature definitions in the low k materials. The hardmask is resistant to damage and deformation. The hardmask also protects the underlying low k materials during subsequent material deposition and planarization or material removal processes to reduce defect formation and feature deformation.

[0012] Also, conventional hardmask materials do not have sufficient selectivity to oxide or metal during polishing, which may result in premature removal of the hardmask and expose the underlying material to the process. The exposed underlying low k dielectric material may be damaged and result in surface defects and feature deformation. Additionally, hardmasks and ARC materials may remain as part of the structure after the underlying dielectric layer is etched and contribute to the structure's overall dielectric constant. Conventional hardmask materials often have high dielectric constants of 7 or greater, which can produce dielectric stacks having a higher than desired dielectric constant. Current hardmask materials have not satisfactorily produced both low k material and sufficient polishing selectivity to be used in damascene fabrication.

[0013] Hardmask and ARC material formed from conventional material may exhibit a porous surface. The small holes are referred to as pinholes. The pinholes can be formed completely through the ARC layer thereby exposing photoresist material deposited on the ARC layer to material underlying the ARC layer, such as silicon nitride. Nitrogen from silicon nitride or other nitrogen containing material may diffuse through the ARC layer and chemically alter the composition of the photoresist material and result in photoresist poisoning.

[0014] Further, as the device size shrinks to 0.13 μm or below and chipmakers migrate to dual damascene process for faster and higher-level performance, new lithographic challenges arise. As the photolithographic patterning wavelength is reduced to 193 nm for forming features of 0.13 μm or below, new photoresists (PR) are being developed to work in conjunction with photolithography at a wavelength of 193 nm. Amine radicals (NH_2) from current dielectric antireflective coatings, such as SiO_xN_y , neutralize the acid catalyst in 193 nm PR. Footing results because the neutralized portion of PR is insoluble in developer. The use of the shorter 193nm wavelength also results in the substrate being more reflective, and increases the difficulty in controlling critical dimensions variations (CD swing), and effective photolithographic processing requires substrate reflectivity below 1 percentage for the shorter wavelengths.

[0015] Dual damascene process presents additional challenges for control of CD swing. For example, Al interconnect processing consists of blanket Al layer deposition, photolithography process to pattern an Al layer, and dielectric gap fill. The high reflectivity and absorption of Al layers of the DUV wavelength does not allow any DUV light to transmit through the Al layers. Thus, the various structures underlying an Al layer do not contribute to any reflection above the Al layer. In contrast, for dual damascene process, the oxide-like low k dielectric is transparent at the patterning wavelength so that the substrate reflection varies depending on the underlying structure. Additionally, anti-reflective layers require dual damascene applications to have sufficient interlayer adhesion with low k inter-metal dielectric materials (IMD). Current anti-reflective coating materials and processes have not been satisfactory in meeting these requirements.

[0016] Therefore, there remains a need for an improved process and material for forming dielectric materials suitable as anti-reflective coatings or hardmasks with a satisfactory etching selectivity for damascene applications.

SUMMARY OF THE INVENTION

[0017] Aspects of the invention generally provide a method for depositing a nitrogen-free dielectric layer for use as a hardmask or anti-reflective coating. In one aspect, the invention provides a method for processing a substrate including introducing a processing gas comprising an oxygen-free silane-based compound and an oxygen and carbon containing compound to the processing chamber and reacting the processing gas to deposit a nitrogen-free dielectric material on the substrate, wherein the dielectric material comprises silicon and oxygen.

[0018] In another aspect of the invention, a method is provided for processing a substrate including depositing at least one dielectric layer on a substrate surface, forming a hardmask layer on the at least one organic or inorganic layer, wherein the hardmask layer is deposited by a process comprising reacting a processing gas comprising an oxygen-free silane-based compound and an oxygen and carbon containing compound to deposit a nitrogen-free dielectric material on the substrate, wherein the hardmask layer comprises silicon and oxygen and has a selectivity of oxide to hardmask of about 4:1 or greater, defining a pattern in at least one region

of the hardmask layer, and forming a feature definition in the at least one organic or inorganic layer by the pattern formed in the at least one region of the hardmask layer.

[0019] In another aspect of the invention, a method is provided for processing a substrate including depositing a first anti-reflective layer and depositing a second anti-reflective layer on the first anti-reflective layer, with the second anti-reflective layer deposited by a process including introducing a processing gas comprising an oxygen-free silane-based compound and an oxygen and carbon containing compound to the processing chamber and reacting the processing gas to deposit a nitrogen-free dielectric material on the substrate, wherein the nitrogen-free dielectric material comprises at least silicon and oxygen.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] So that the manner in which the above features of the invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

[0021] It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0022] Figure 1 is a cross sectional view showing a dual damascene structure comprising a nitrogen free anti-reflective coating as described herein.

[0023] Figures 2A-2H are cross sectional views showing one embodiment of a dual damascene deposition sequence.

[0024] Figures 3A-3G are cross sectional views showing one embodiment of a dual damascene deposition sequence.

[0025] Figure 4 is a schematic diagram of a dual layer antireflective coating indicating light reflection.

[0026] Figure 5 is a chart indicating the relationship between the gas flow ratio of $\text{SiH}_4/\text{N-free}$ and extinction coefficient.

[0027] Figure 6 shows the results of post oxygen ashing extinction coefficient reduction as a function of process conditions.

[0028] Figure 7 shows the extinction coefficient change after 9 day shelf life monitoring.

[0029] Figure 8 shows compressive stress as a function of process conditions.

[0030] For a further understanding of aspects of the invention, reference should be made to the ensuing detailed description.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0031] Aspects of the invention described herein refer to methods for depositing a nitrogen-free dielectric material. The nitrogen-free dielectric material may be used as an anti-reflective coating adjacent to a dielectric material or a hardmask dielectric layer in a metallization scheme for a damascene or dual damascene process.

[0032] In one aspect, the nitrogen-free dielectric material may be deposited by reacting a processing gas comprising a silane-based compound and an oxygen and carbon containing compound, such as carbon dioxide or an organosilicon compound. The nitrogen-free dielectric material comprises at least silicon and oxygen, and may further include carbon. The nitrogen-free dielectric material may be deposited by a plasma-enhanced chemical vapor deposition process. The deposited nitrogen-free dielectric material may exhibit a dielectric constant of about 11 or less, such as about 4 or less.

[0033] Suitable silane-based compounds for the processes described herein include oxygen-free silane-based compounds. Oxygen-free silane-based compounds may have the formula $\text{Si}_x\text{H}_{2x+2}$, $\text{Si}_x\text{H}_y\text{Cl}_z$, $(\text{CH}_3)_z\text{Si}_x\text{H}_y$, or combinations thereof may be used in the deposition processes described herein, X may be equal to 1 to 4, Y may be equal to $2X + 1$, and Z may be equal to 1 to $2X + 2$. Examples of such compounds include silane, disilane, chlorosilane, dichlorodisilane,

hexachlorosilane, methylsilane, dimethylsilane, trimethylsilane, tetramethylsilane, and combinations thereof. One or more of the oxygen-free silane-based compounds may be used in the deposition processes described herein. The silane-based compound, such as silane, may be supplied to a plasma processing chamber at a flow rate between about 100 sccm and about 700 sccm.

[0034] Suitable oxygen and carbon containing compounds include carbon dioxide, carbon monoxide, and organosilicon compounds that contain oxygen. Suitable organosilicon compounds that contain oxygen include tetraethoxysilane (TEOS), triethoxyfluorosilane (TEFS), 1,3,5,7-tetramethylcyclotetrasiloxane (TMCTS), dimethyldiethoxysilane, dimethyldimethoxysilane, 1,3-dimethyldisiloxane, 1,1,3,3-tetramethyldisiloxane (TMDSO), hexamethyldisiloxane (HMDS), 1,3-bis(silanomethylene)disiloxane, bis(1-methyldisiloxanyl)methane, 2,2-bis(1-methyldisiloxanyl)propane, hexamethoxydisiloxane (HMDOS), 1,3,5-trisilano-2,4,6-trimethylene, octamethylcyclotetrasiloxane (OMCTS), 1,3,5,7,9-pentamethylcyclopentasiloxane, 1,3,5,7-tetrasilano-2,6-dioxy-4,8-dimethylene, hexamethylcyclotrisiloxane, and combinations thereof.

[0035] The organosilicon compounds are used to provide a source of oxygen and carbon for the deposited nitrogen-free dielectric material. Liquid oxygen-containing organosilicon compound, such as TEOS, may be vaporized and supplied to the plasma processing chamber at a flow rate of about 2000 mgm or greater. The oxygen-free silane-based compounds and the liquid organosilicon compounds are generally supplied to the processing chamber in a flow rate ratio of the oxygen-free silane-based compound to the liquid oxygen containing organosilicon compound between about 1 (sccm):20 (mgm) and about 6 (sccm):5 (mgm).

[0036] Other materials that may provide oxygen and carbon sources, such as carbon monoxide and carbon dioxide, may be used with the organosilicon compounds, or used as an alternative to the organosilicon compounds.

[0037] If oxygen-containing organosilicon compounds are reacted to deposit the nitrogen-free dielectric material, the nitrogen-free dielectric material has an oxygen content between about 15 atomic percentage and about 50 atomic percentage, for

example, between about 15 atomic percentage and about 30 atomic percentage to have sufficient layer properties to perform an anti-reflective coating or hardmask layer. The silicon content of the deposited film may contain between about 20 atomic percentage and about 50 atomic percentage, between about 20 and about 30 atomic percentage of hydrogen, and generally less than about 15 atomic percentage of carbon. The film is generally considered a carbon-doped silicon oxide at the respective silicon, oxygen, and carbon atomic percentages described herein.

[0038] The amount of oxygen, silicon, and carbon content of the deposited film may vary. For example, increasing silane-base precursor flow rates have been observed to result in reducing the oxygen content of the deposited materials.

[0039] The processing gas may further comprise an inert gas. Inert gases, such as a noble gas selected from the group of argon, helium, neon, xenon, or krypton, and combinations thereof, may be added to the processing gas to improve processing stability. The inert gas may be provided at a flow rate between about 100 sccm and about 20,000 sccm.

[0040] The processes described herein are preferably performed in a processing chamber adapted to chemically mechanically deposit organosilicon material while applying RF power, such as a DxZ™ chemical vapor deposition chamber or the Producer™ deposition chamber, both of which are commercially available from Applied Materials, Inc., Santa Clara, California. An example of a CVD reactor that may be used with the processes herein is described in U.S. Patent 5,000,113, entitled A Thermal CVD/PECVD Reactor and Use for Thermal Chemical Vapor Deposition of Silicon Dioxide and *In-situ* Multi-step Planarized Process, issued to Wang *et al.* and assigned to Applied Materials, Inc., the assignee of the present invention.

[0041] A nitrogen-free dielectric material may be deposited in one embodiment by supplying the silane-based compound, such as silane, to a plasma processing chamber at a flow rate between about 100 sccm and about 700 sccm, supplying the oxygen-containing organosilicon compound, such as TEOS, to the plasma

processing chamber at a flow rate of about 2000 mgm or greater, supplying a noble gas at a flow rate between about 100 sccm and about 20,000 sccm, maintaining a substrate temperature between about 100°C and about 1000°C, maintaining a chamber pressure below about 50 Torr and an RF power of between about 0.16 watts/cm² and about 32 watts/cm², or a power level between about 50 watts and about 10,000 watts for a 200 mm substrate. The substrate is maintained at a distance between about 0.1 cm and about 10 cm from the source of the processing gas.

[0042] The RF power can be provided at a frequency between about 1 kHz and about 10 GHz. In one aspect, the RF power can be provided at a high frequency such as between about 13 MHz and about 14 MHz or a mixed frequency of the high frequency and the low frequency, for example, a high frequency of about 13.56 MHz and a low frequency of about 356 KHz. The RF power can be provided continuously or in short duration cycles wherein the power is on at the stated levels for cycles less than about 200 Hz and the on cycles total between about 10 percentage and about 30 percentage of the total duty cycle. The processing gas may be introduced into the chamber by a gas distributor, the gas distributor may be positioned between about 200 mils and about 700 mils from the substrate surface. The following chart provides embodiments for use with 200 and 300 mm substrates. The high k DARC deposition is followed by low k DARC deposition.

[0043]

Table 1. Processing Conditions for High and Low k Layer Deposition.

	200 mm			300 mm		
	Low k	High k	Range	Low k	High k	Range
SiH ₄ , sccms	95	109	50-150	198	255	100-350
CO ₂ , sccms	4500	700	300-7000	9000	3000	500-14000
He, sccms	0	3500	0-7000	0	5000	0-10000
T, °C	350	350	250-550	350	350	250-550
P, Torr	6	5.5	4.5-8	6	5.5	4.5-8
Spacing, mils	530	485	230-600	520	510	230-600
13.56 MHz RF, W	125	210	50-400	245	200	50-800
356 KHz RF, W	0	0	0-100	0	0	0-200

[0044] In one preferred aspect, a nitrogen-free dielectric material may be deposited in one embodiment by supplying silane to a plasma processing chamber at a flow rate between about 100 sccm and about 700 sccm, supplying TEOS to the plasma processing chamber at a flow rate of about 2000 mgm or greater, supplying helium at a flow rate between about 500 sccm and about 10,000 sccm, maintaining a substrate temperature between about 250°C and about 450°C, maintaining a chamber pressure between about 3 Torr and about 10 Torr, supplying an RF power of between about 100 watts and about 1000 watts for a 200 mm substrate, and spacing the substrate from the source of processing gas at a distance between about 300 mils and about 500 mils.

[0045] The above process parameters provide a deposition rate for the nitrogen-free dielectric material in the range of about 500 Å/min to about 20,000 Å/min, such as at about 2000 Å/min, when implemented on a 200 mm (millimeter) substrate in a deposition chamber available from Applied Materials, Inc., Santa Clara, California.

[0046] Following deposition, the deposited dielectric material may be annealed at a temperature between about 100°C and about 400°C for between about 1 minute and about 60 minutes, preferably at about 30 minutes, to reduce the moisture content and increase the solidity and hardness of the dielectric material, if desired. Annealing is preferably performed after the deposition of a subsequent layer to

reduce or minimize any shrinkage or deformation of the dielectric layer that may occur during annealing. Inert gases, such as argon and helium, may be added to the annealing atmosphere.

[0047] The deposited nitrogen-free dielectric material may be plasma treated to remove contaminants or otherwise clean the exposed surface of the nitrogen-free dielectric layer prior to subsequent deposition of materials thereon. The plasma treatment may be performed in the same chamber used to deposit the nitrogen-free dielectric material. The plasma treatment generally includes providing an inert gas including helium, argon, neon, xenon, krypton, or combinations thereof, of which helium is preferred, or a reducing gas including hydrogen, ammonia, and combinations thereof, to a processing chamber. The plasma treatment may be performed between about 10 seconds and about 100 seconds. The plasma treatment is believed to clean contaminants from the exposed surface of the nitrogen-free dielectric material and may be used to stabilize the layer, such that it becomes less reactive with moisture or oxygen under atmospheric condition as well as the adhesion of layers formed thereover.

[0048] However, it should be noted that the respective parameters might be modified to perform the plasma processes in various chambers and for different substrate sizes, such as 300 mm substrates. An example of a plasma treatment for dielectric films is further disclosed in U.S. Patent Application Serial No. 09/336,525, entitled, "Plasma treatment to Enhance adhesion and to Minimize Oxidation of Carbon-Containing Layers," filed on June 18, 1999, and in co-pending U.S. Patent Application Serial No. 10/122,106, filed on April 11, 2002, entitled, "Methods for Depositing Dielectric Materials", both of which are incorporated herein by reference to the extent not inconsistent with the claimed aspects and description herein.

[0049] The deposited nitrogen-free dielectric material may have a light absorption coefficient, or extinction coefficient (κ). The κ value represents the amount of absorption of light passing therethrough. As the κ value increases, the amount of light absorption increases. A material having a κ value of greater than about 0.5 has been observed to be effective for use as a hardmask and κ values

between about 0 and about 2 may be used for ARC applications depending upon the requirements for use of the ARC layer. The extinction coefficient can be varied between about 0 to about 2.0, such as between about 0 and about 1.5, for example between about 0.1 and about 1.1, at wavelengths below about 250 nm (nanometers), such as about 248 nm wavelengths or 193 nm wavelengths, making it suitable for use as an anti-reflective coating (ARC) at deep ultraviolet (DUV) wavelengths.

[0050] When the dielectric is transparent to 193 nm radiation, an absorbing ARC ($\kappa > 1$, thickness > 1000) may be helpful. Antireflective coating minimizes the substrate reflectivity to make a precise pattern transfer from a mask to photoresist.

[0051] The nitrogen-free dielectric material also has an index of refraction (n), which represents the refraction of the light passing therethrough, of less than about 3 at wavelengths below about 250 nm, such as at 193 nm wavelength light. Generally, n values, such between about 1.5 and about 2.2, for example, between about 1.7 and about 2.2, are acceptable for lithographic processes at wavelengths below 250 nm (nanometers) using the hardmask and ARC layer applications described herein. The n values have been observed to generally increase with the κ value up to about a κ value of about 0.5. The n values are then observed to generally decrease as κ values increase above 0.5.

[0052] The extinction coefficient (κ) and the index of refraction (n) of the nitrogen-free dielectric material may be varied as a function of the composition of the gas mixture and processing parameters. It is believed that the amount of Si-H bonds in the deposited material affects the extinction coefficient (κ), and that modification of compositions and processing parameters will allow for control of the amount of Si-H bonds and the optical properties of the deposited material.

[0053] It has been observed that increasing the silicon concentration in the deposited material results in increased Si-H bonds in the deposited material and increased κ values of the deposited material. In contrast, an increase in the oxygen content of the deposited material results in a decreased κ value. Increasing the

carbon concentration of the deposited material has also been observed to increase the κ value.

[0054] As the concentration of the silane-source gas is increased, *i.e.*, the ratio of silane to TEOS increases, the amount of Si-H bonds and the extinction coefficient (κ) of the deposited material is observed to increase. For example, as the silane flow rate increases from about 50 to about 225 sccm at a constant TEOS flow rate of about 500 mgm, the κ value increases from about 0.3 to about 0.9 when all other values are held constant. In another example, as the silane flow rate is increased from about 150 sccm to about 550 sccm at a constant TEOS flow rate of 2000 mgm, the κ value increases from about 0.275 to about 0.625 when all other values are held constant. Increasing the silane-based precursor flow rates has been observed to result in reducing the oxygen content of the deposited materials.

[0055] The index of refraction (n) may also be tailored by controlling the ratio of silane to TEOS. For example, a silane flow rate between about 50 sccm and about 250 sccm at a 500 mgm flow rate of TEOS can control the n value between about 1.90 and about 2.05, while a silane flow rate between about 150 sccm and about 550 sccm at a 2000 mgm flow rate of TEOS can control the n value between about 1.85 and about 1.70 respectively.

[0056] The κ values and n values may also be controlled by power levels and pressures. For example, increasing power has been generally observed to increase the oxygen content of deposited material and the κ value. Additionally, increasing deposition pressure has also been observed to result in lower κ values.

[0057] The nitrogen-free dielectric material is suitable for deposition on organic materials, such as dielectric silicon carbide or silicon oxycarbide films, or inorganic materials, such as polysilicon or metals' materials including copper or barrier materials, such as tantalum. The embodiments described herein for depositing nitrogen-free dielectric material are provided to illustrate the invention and particular embodiments, and should not be used to limit the scope of the invention.

Deposition of an ARC Layer for a Dual Damascene Structure

[0058] An example of a damascene structure that is formed using the nitrogen-free dielectric material described herein as a barrier layer is shown in Figure 1. A barrier layer 110, such as silicon carbide or oxygen-doped silicon carbide may be deposited to reduce or minimize interlayer diffusion of material. An example of a silicon carbide deposition process is described in co-pending U.S. Patent Application Publication No. 2003/008992, filed on October 1, 1998, entitled, "Silicon Carbide Deposition As A Barrier Layer And An Etch Stop", and in co-pending U.S. Patent Application Publication No. 2003/0194496, filed on April 11, 2002, entitled, "Methods for Depositing Dielectric Materials", both of which are incorporated herein by reference to the extent not inconsistent with the claimed aspects and description herein. The substrate surface may comprise metal features 107 formed in a dielectric material 105.

[0059] A first dielectric layer 112, typically a low k interlayer dielectric material, such as a silicon oxycarbide material (carbon doped silicon oxide) produced by oxidizing an alkylsilane in a RF energy-enhanced chemical vapor deposition process, is deposited on the oxygen-doped silicon carbide barrier layer 110 on the substrate surface including metal features 107 formed in a dielectric material 105. An example of the dielectric material for the first dielectric layer 112 and process for deposition of the dielectric material is more fully described in U.S. Patent No. 6,287,990, issued on September 11, 2001, which is incorporated by reference herein to the extent not inconsistent with the description and claims herein.

[0060] An etch stop (or second barrier layer) 114, for example, a low k silicon carbide material, is then deposited on the first dielectric layer 112. The etch stop 114 is then pattern etched to define the openings of an interconnect or contact/via 116. A second dielectric layer 118, which may have the same composition of the first dielectric layer 112 is then deposited over the patterned etch stop. A nitrogen-free ARC layer 119 as described herein is then deposited over the second dielectric layer 118. A photoresist is then deposited and patterned by conventional means known in the art to define the contacts/via 116. A single etch process is then

performed to define the contact/vias 116 down to the etch stop and to etch the unprotected dielectric exposed by the patterned etch stop to define the contacts/vias 116. One or more conductive materials 120 such as copper are then deposited to fill the formed contacts/vias 116.

[0061] A preferred dual damascene structure fabricated in accordance with the invention including a nitrogen-free ARC layer deposited by the processes described herein is sequentially depicted schematically in Figures 2A-2H, which are cross sectional views of a substrate having the steps of the invention formed thereon.

[0062] As shown in Figure 2A, an oxygen-doped silicon carbide barrier layer 110 is deposited on the substrate surface. An example of a oxygen-doped silicon carbide deposition is as follows; introducing 1,3,5,7-tetramethylcyclotetrasiloxane (TMCTS) at about 300 mgm into the processing chamber, introducing trimethylsilane (TMS) at about 360 mgm into the processing chamber, introducing helium at about 1000 sccm into the processing chamber, generating a plasma in the processing chamber by applying 950 watts of RF energy, maintaining the substrate temperature at about 350°C, maintaining the chamber pressure at about between about 8.7 Torr to deposit an oxygen-doped silicon carbide layer. The spacing between the gas distributor and the substrate surface is about 515 mils. The above provided example is merely illustrative and should not be construed or interpreted as limiting the scope of the invention.

[0063] Further examples of depositing oxygen-doped silicon carbide material are more fully described in U.S. Patent Application Publication No. 2003/0113995, filed on March 12, 2002, entitled, "Method for Depositing a Low K Dielectric Film for Hardmask Application," which is incorporated herein by reference to the extent not inconsistent with the claimed aspects and description herein. While not shown, a capping layer of nitrogen-free silicon carbide may be deposited on the barrier layer 110. The nitrogen-free silicon carbide capping layer may be deposited *in situ*.

[0064] The oxygen-doped silicon carbide barrier layer 110 may be plasma treated with an inert gas including helium (He), argon (Ar), neon (Ne), and combinations thereof, and/or a reducing gas including hydrogen, ammonia, and

combinations thereof. The plasma treatment may be performed *in situ* with the deposition of the oxygen-doped silicon carbide material.

[0065] A first dielectric layer 112 of interlayer dielectric material, such as a silicon oxycarbide, is deposited on the first oxygen-doped silicon carbide barrier layer 110 to a thickness of about 5,000 to about 15,000 Å, depending on the size of the structure to be fabricated. Example of a low dielectric constant material that may be used as an interlayer dielectric material is Black Diamond™ commercially available from Applied Materials, Inc., of Santa Clara, California. The first dielectric layer may also comprise other low k dielectric materials including a low polymer material, such as paralyne, or a low k spin-on glass such as un-doped silicon glass (USG) or fluorine-doped silicon glass (FSG).

[0066] The first dielectric layer 112 may then be treated by a plasma process to remove contaminants and densify the surface of the dielectric layer 122. An example of a plasma process includes introducing a processing gas containing helium or a reducing gas, such as hydrogen, between about 500 sccm and about 1,500 sccm, at a power level of between about 600 watts and about 800 watts for between about 40 seconds and about 60 seconds for a 200 millimeter substrate. The processing chamber is maintained at a pressure of about 20 Torr or less and at a substrate temperature of about 450°C or less during the reactive clean process.

[0067] As shown in Figure 2B, the low k etch stop 114, which may be a silicon carbide material, is then deposited on the first dielectric layer to a thickness of about 200 to about 1000 Å. The low k etch stop 114 may be plasma treated as described herein for the oxygen-doped silicon carbide barrier layer 110. The low k etch stop 114 is then pattern etched to define the contact/via openings 116 and to expose first dielectric layer 112 in the areas where the contacts/vias are to be formed as shown in Figure 2C. Preferably, the low k etch stop 114 is pattern etched using conventional photolithography and etch processes using fluorine, carbon, and oxygen ions. While not shown, a nitrogen-free silicon carbide or silicon oxide cap layer between about 100 Å and about 500 Å thick may be deposited on the etch stop 116 prior to depositing further materials.

[0068] After low k etch stop 114 has been etched to pattern the contacts/vias and the photoresist has been removed, a second dielectric layer 118 of silicon oxycarbide is deposited to a thickness of about 5,000 to about 15,000 Å and a nitrogen-free ARC layer 119 is deposited thereon as shown in Figure 2D. The second dielectric layer 118 may be plasma treated as described herein for the first dielectric layer 112 prior to depositing the nitrogen-free ARC layer 119. The plasma treatment is believed to reduce the reactivity of the surface of the layer 118 to subsequently deposited materials.

[0069] The nitrogen-free ARC layer 119 may be deposited as described herein on the second dielectric layer 118. For example, the ARC layer 110 may be deposited by supplying silane to a plasma processing chamber at a flow rate between about 100 sccm and about 700 sccm, supplying TEOS to the plasma processing chamber at a flow rate of about 2000 mgm or greater, supplying helium at a flow rate between about 500 sccm and about 10,000 sccm, maintaining a substrate temperature between about 250°C and about 450°C, maintaining a chamber pressure between about 3 Torr and about 10 Torr, supplying an RF power of between about 100 watts and about 1000 watts for a 200 mm substrate, and spacing the substrate from the source of processing gas at a distance between about 300 mils and about 500 mils.

[0070] In an alternative embodiment, a nitrogen-free silicon carbide or silicon oxide cap layer between about 100 Å and about 500 Å thick may be deposited on second dielectric layer 118 prior to depositing additional materials, such as the ARC layer 119.

[0071] A photoresist material 122 is then deposited on the nitrogen-free ARC layer 119 and patterned preferably using conventional photolithography processes to define the interconnect lines 120 as shown in Figure 2E. The photoresist material 122 comprises a material conventionally known in the art, preferably a high activation energy photoresist, such as UV-5, commercially available from Shipley Company Inc., of Marlborough, Massachusetts. The interconnects and contacts/vias are then etched using reactive ion etching or other anisotropic etching techniques to define the metallization structure (*i.e.*, the interconnect and contact/via) as shown in

Figure 2F. Any photoresist or other material used to pattern the etch stop 114 or the second dielectric layer 118 is removed using an oxygen strip or other suitable process.

[0072] The metallization structure is then formed with a conductive material such as aluminum, copper, tungsten or combinations thereof. Presently, the trend is to use copper to form the smaller features due to the low resistivity of copper ($1.7 \text{ m}\Omega\text{-cm}$ compared to $3.1 \text{ m}\Omega\text{-cm}$ for aluminum). Preferably, as shown in Figure 2G, a suitable barrier layer 124 such as tantalum nitride is first deposited conformally in the metallization pattern to prevent copper migration into the surrounding silicon or dielectric material. Thereafter, copper 126 is deposited using either chemical vapor deposition, physical vapor deposition, electroplating, or combinations thereof to form the conductive structure. Once the structure has been filled with copper or other metal, the surface is planarized using chemical mechanical polishing, as shown in Figure 2H.

[0073] The deposition of the nitrogen-free dielectric materials as the anti-reflective coating was observed to eliminate any adverse interactions between the NH_2 amine group from nitrogen containing dielectric materials and the DUV 193 nm photoresist that is directly in contact with the anti-reflective coating (ARC), and thus, eliminate major source of photoresist poisoning-induced footing. The nitrogen-free dielectric ARC demonstrated a wide tunable range of its optical properties at 193nm in a single wafer PECVD reactor: $1.6 < n < 1.9$ and $0 < \kappa < 1.1$. This range enables cost-effective and *in-situ* deposition of a dual-layer dielectric ARC on the low k dielectric layers during the dual damascene process. Nitrogen-free dielectric ARC can be integrated with low k dielectrics and has sufficient adhesion with low k materials as well as the ability to be etched and chemically and mechanically polished together with low k dielectrics.

Deposition of a Dual Damascene Structure

[0074] In an alternative embodiment of the damascene structure, the nitrogen-free dielectric material described herein may be deposited as a hardmask layer over a dielectric layer prior to depositing the photoresist material for improving damascene formation and protecting the low k material of the damascene structure

when etching the metallization structure. An example of a damascene structure that is formed using a nitrogen-free dielectric material as a hardmask described herein is shown in Figures 3A-G, which are cross sectional views of a substrate having the steps of the invention formed thereon.

[0075] As shown in Figure 3A, a barrier layer 310, such as silicon carbide, is deposited on the substrate surface to eliminate inter-level diffusion between the substrate and subsequently deposited material. The substrate surface may comprise feature definitions 307 formed in a dielectric material 305. The barrier layer 310 may be doped with oxygen, boron, phosphorus, or combinations thereof.

[0076] A first dielectric layer 312, which may comprise a silicon oxycarbide material is deposited on the barrier layer 310 on the substrate surface and in feature definitions 307 formed in a dielectric material 305. The first dielectric layer 312 of interlayer dielectric material is deposited on the barrier layer 310 by oxidizing an organosilane or organosiloxane, such as trimethylsilane, to a thickness of about 5,000 to about 15,000 Å, depending on the size of the structure to be fabricated.

[0077] Examples of a low dielectric constant material that may be used as an interlayer dielectric material is Black Diamond™ commercially available from Applied Materials, Inc., of Santa Clara, California. Alternatively, the first dielectric layer may also comprise other low k dielectric material such as a low k polymer material including paralyne or a low k spin-on glass such as un-doped silicon glass (USG) or fluorine-doped silicon glass (FSG). A plasma process following deposition as described herein for the silicon oxycarbide layer may then treat the first dielectric layer 312.

[0078] A low k etch stop (or second barrier layer) 314, such as a silicon carbide material or oxidized organosilane layer, is then deposited on the first dielectric layer 312 to a thickness of about 200 to about 1000 Å. The low k etch stop 314 is then pattern etched to define the contact/via openings 316 and to expose first dielectric layer 312 in the areas where the contacts/vias are to be formed as shown in Figure 3A. Preferably, the low k etch stop 314 is pattern etched using conventional photolithography and etch processes using fluorine, carbon, and oxygen ions. While

not shown, a nitrogen-free silicon carbide or silicon oxide cap layer between about 100 Å and about 500 Å thick may be deposited on the etch stop 316 prior to depositing further materials.

[0079] After the low k etch stop 314 has been etched to pattern the contacts/vias and the photoresist has been removed, a second dielectric layer 318, such as silicon oxycarbide, is deposited to a thickness of about 5,000 to about 15,000 Å as shown in Figure 3A. The second dielectric layer 318 may also be plasma treated as described herein.

[0080] A nitrogen-free dielectric hardmask layer 322 as described herein may then be deposited on the second dielectric layer 318 and patterned preferably using conventional photolithography processes to define the interconnect lines 320 as shown in Figure 3B. The nitrogen-free dielectric hardmask layer 322 is a hardmask which may perform as a stop for chemical mechanical polishing techniques to allow removal of conductive material while protecting low k dielectric materials, such as the second dielectric layer 318, from damage during etching processes or from polishing processes, such as chemical-mechanical polishing. The hardmask layer 322 of the nitrogen-free dielectric material described herein has exhibited an etching selectivity of oxide or metal to hardmask of about 4:1 or greater, and in some instances has exhibited an etching selectivity of about 10:1 or greater of oxide or metal to hardmask.

[0081] The nitrogen-free dielectric hardmask layer 322 is deposited as described herein. An example of a hardmask deposition includes supplying silane to a plasma processing chamber at a flow rate between about 100 sccm and about 700 sccm, supplying TEOS to the plasma processing chamber at a flow rate of about 2000 mgm or greater, supplying helium at a flow rate between about 500 sccm and about 10,000 sccm, maintaining a substrate temperature between about 250°C and about 450°C, maintaining a chamber pressure between about 3 Torr and about 10 Torr, supplying an RF power of between about 100 watts and about 1000 watts for a 200 mm substrate, and spacing the substrate from the source of processing gas at a distance between about 300 mils and about 500 mils. The hardmask 322 is

deposited at a deposition rate of about 2000 Å/min. The hardmask 322 was observed to have an etch selectivity of oxide or metal to hardmask of about 10:1.

[0082] The features are then etched through to the second dielectric layer 318, the low k etch stop 314, the first dielectric layer 312, and the silicon carbide barrier layer 310 as shown in Figure 3C. The hardmask 322 may be completely removed by the etch process.

[0083] The interconnect lines 320 are then filled to form a metallization structure with a conductive material such as aluminum, copper, tungsten or combinations thereof. Presently, the trend is to use copper to form the smaller features due to the low resistivity of copper ($1.7 \mu\Omega\text{-cm}$ compared to $3.1 \mu\Omega\text{-cm}$ for aluminum). Preferably, as shown in Figure 3D, a suitable barrier layer 324 such as tantalum or tantalum nitride is first deposited conformally in the metallization pattern to prevent copper migration into the surrounding silicon or dielectric material. Thereafter, copper 326 is deposited using electrochemical deposition, such as electroplating or electroless deposition, chemical vapor deposition, physical vapor deposition, or combinations thereof, to fill the structure as shown in Figure 3E.

[0084] Once the structure has been filled with copper or other metal, the surface is planarized using chemical mechanical polishing. However, the polishing resistant nitrogen-free dielectric hardmask layer 322 may remain behind after the polishing process as shown in Figure 3F. The nitrogen-free dielectric hardmask layer 322 may be removed by a plasma process from the surface of the substrate.

Deposition of a Dual ARC Layer

[0085] The nitrogen-free dielectric ARC layer described herein may be deposited as a dual layer (bilayer) prior to depositing and patterning of a photoresist thereon. Referring to Figure 4, in the dual layer format 400, a bottom absorption layer 410 with a high index on infraction (n) and a high extinction coefficient (κ) is provided to act as a reflector as well as absorber while thickness and optical properties of a top phase-shift layer (low k layer) 420 are engineered to cancel the reflected light from the resist 440/top layer 420 interface and top layer (low k) 420/bottom layer (high k)

410 interface. The dual layers 410, 420 are deposited on a low k material, such as a carbon-doped silicon oxide as described herein. A photoresist material 440 is then deposited on the top layer prior to photolithography

[0086] The top layer 420 and bottom layers 410 may be deposited in situ and from the same precursors in the chamber. The nitrogen-free dielectric deposition herein may have processing parameters varied, such as temperature, pressure, relative amounts or ratio of precursors to provide independent optical properties for the top layer 420 and bottom layers 410. The dual layer coating 400 is typically designed to provide a substrate reflectivity below 1 percentage across the wafer, which minimizes CD swing. Alternatively, only the top layer 420 or bottom layer 410 may comprise the nitrogen free dielectric ARC material described herein, with the other layer comprising a conventional ARC material.

Deposition Examples

[0087] The following examples illustrate deposition of the materials described herein for ARC and hardmask applications. The materials were deposited using a chemical vapor deposition chamber that is part of an integrated processing platform. In particular, the films were deposited using a Producer™ deposition system commercially available from Applied Materials, Inc. of Santa Clara, California.

[0088] A nitrogen-free ARC layer was deposited by a mixed precursor process on a 200 mm substrate from the following reactive gases at a chamber pressure of about 5 Torr and substrate temperature of about 400°C.

Silane (SiH₄), at about 400 sccm;

Tetraethoxysilane (TEOS), at about 2000 mgm; and

Helium, at about 2,000 sccm;

[0089] The substrate was positioned about 400 mils from the gas distribution showerhead. A plasma was generated by applying a power level of about 500 W at a frequency of 13.56 MHz to the showerhead. The film was deposited at a rate of about 3168 Å/min for about 10 seconds for a deposition thickness of about 528 Å.

The deposited film was tested and optical properties of an absorption coefficient (κ) of about 0.369 and a n value of 1.776 for a 193 nm wavelength was observed.

[0090] A nitrogen-free hardmask layer was deposited by a mixed precursor process on a 200 mm substrate from the following reactive gases at a chamber pressure of about 5 Torr and substrate temperature of about 400°C.

Silane (SiH_4), at about 375 sccm;

Tetraethoxysilane (TEOS), at about 1000 mgm; and

Helium, at about 2,000 sccm;

[0091] The substrate was positioned about 400 mils from the gas distribution showerhead. A plasma was generated by applying a power level of about 500 W at a frequency of 13.56 MHz to the showerhead. The film was deposited at a rate of about 3898 Å/min for about 10 seconds for a deposition thickness of about 650 Å. The deposited film was tested and optical properties of an absorption coefficient (κ) of about 1.017 and a n value of 1.774 for a 193 nm wavelength was observed.

Dual Layer Coating Examples

[0092] Sample nitrogen-free dielectric anti-reflective coatings were deposited in a parallel plate plasma-enhanced chemical vapor deposition (PECVD) at $T = 350^\circ\text{C}$ using silane (SiH_4) and an nitrogen-free oxidizer. A Thermawave Optiprobe, model-5340 was used to measure thickness, n and κ values at $\lambda = 193\text{nm}$. Process parameters such as high frequency power, pressure, gas ratio and susceptor spacing were varied to explore the tunable range of optical properties. A Prolith reflectivity simulator, which can calculate the substrate reflectivity as a function of up to two variables of an ARC film for a given film stack with known optical properties and thickness, was used to find sets of optimal n, κ , and thickness for minimum substrate reflectivity given a film stack. The composition of the nitrogen-free dielectric anti-reflective films was analyzed by Rutherford Back Scattering method (RBS), Hydrogen Forward Scattering (HFS), and Nuclear Reaction Analysis (NRA). A Bio-Rad FTIR Model QS-312 was used to study chemical bonding of the deposited layers. The nitrogen free dielectric coating with a low κ dielectric SiOCH

was tested using m-ELT by depositing 500Å-800Å of nitrogen-free dielectric ARC on 5kÅ of SiOCH. The nitrogen-free dielectric ARC was etched in e-Max™ chamber, Applied Materials' dielectric etcher, with CF₄ chemistry that is used for silicon oxycarbide or carbon-doped silicon oxide (SiOCH) trench etch and chemically-mechanically polished in a CMP chamber.

[0093] The nitrogen-free precursors in PECVD processing ensured that the anti-reflective coating did not have nitrogen, as confirmed by RBS/HFS/NRA. No photoresist poisoning was observed, indicating that the NH₂ amine group in ARC is minimized or eliminated.

[0094] Referring to Figure 5, the n and κ of the nitrogen free dielectric ARC have ranges wide enough to cover a dual-layer ARC, minimizing reflectivity below 1 percentage. Among the process knobs available in a PECVD reactor, gas flow ratio of SiH₄/nitrogen free oxidizer is the simplest parameter to vary n and κ. As more SiH₄ flows, κ consistently increases. Interestingly, it was observed that although initially the n increases, it actually then decreases as κ increases beyond 0.6 (see Figure 5). According to RBS/HFS analysis, silicon atom (Si) content and hydrogen atom (H) content increase together with κ value and additionally, the Si-H absorption signal increases according to FTIR spectra, confirming that Si-H bonds are responsible for absorption at DUV wavelengths.

[0095] For 90nm dual damascene processes, barrier materials and low κ IMD are deposited, and patterned with via and trench etch prior to feature fill with a barrier layer and copper electroplating. The optimal sets of n, κ, and thickness for dual layers were obtained using a Prolith simulator for the low κ IMD/barrier stack.

[0096] A set of exemplary reflectivity contour maps were used to test the film. One of the possible sets of results has a top layer having an index of refraction of $n=1.78\pm0.1$, an extinction coefficient of $\kappa=0.3\pm0.05$, and a thickness of $t=250\pm50\text{Å}$, and a bottom layer of having an index of refraction of $n=1.75\pm0.1$, an extinction coefficient of $\kappa=1.0\pm0.1$, and a thickness of $t=400\pm100\text{Å}$. Other optimal sets of n, κ, and thickness values for a top layer and a very wide window for a bottom layer have been observed. The dual-layer scheme offers a much wider n, κ, and thickness

window, providing lower reflectivity than a single layer. These optimal n and κ windows fall within the tuning range of the nitrogen-free dielectric ARC, allowing a flexible integration scheme. In our single wafer PECVD reactor, a low κ top layer can be continuously deposited in-situ following the high κ bottom layer without transferring the wafer from the chamber. The dual-layer nitrogen-free dielectric ARC can thus be readily deposited while maintaining high throughput.

[0097] In dual damascene application, photoresist material may be removed from the ARC coating, typically by an oxygen-based process known as O_2 -ashing, which may be a plasma-based process. The nitrogen-free ARC coating is subjected to repeated photoresist deposition and O_2 -ashing during dual damascene formation and the stability of the film, i.e., retention of optical properties of the ARC layer, needs to be retained under such conditions. A nitrogen-free capping layer, such as an oxide, is deposited on the nitrogen-free ARC coating prior to deposition, patterning, and ashing of a photoresist material by O_2 plasma. The capping layer may be deposited to between about 50Å and about 100Å to protect the nitrogen-free dielectric ARC to retain the ARC layer's optical properties. Film stability may also be improved for low κ nitrogen-free dielectric ARC by a nitrogen-free oxidizing plasma treatment after deposition.

[0098] Interlayer adhesion between the nitrogen-free dielectric ARC and low k IMD films, such as SiOCH, was tested by m-ELT and found to be equivalent to that of a standard SiON dielectric ARC with SiOCH at the same thickness. The nitrogen-free dielectric ARC K_{app} was greater than 0.252 MPa-m^{1/2}. The nitrogen-free dielectric ARC had similar etching properties to that of the dielectric materials, with the same etch chemistry, as the low k IMD via/trench. We measured the etch rate of the N-free dielectric ARC by SiOCH trench etch CF_4 chemistry in the e-Max™, etch chamber. The measured etch rate of the nitrogen-free dielectric ARC by SiOCH trench etch CF_4 chemistry in the e-Max™ etch chamber was at least 20percentage faster than SiOCH (see Table 2). Additionally, the N-free dielectric ARC has a polishing material removal rate comparable to FSG and expected to be faster than that of SiOCH, which has a degree of porosity.

Table 2:

	SiOCH	N-free_low K	N-free_high K	SiON	FSG
Etch Rate($\text{\AA}/\text{m}$)	1	1.2	1.5		
Polish rate($\text{\AA}/\text{m}$)		1.0	1.3	1.1	1

[0099] Figures 6 and 7 illustrate how using a mixture of high and low frequencies produces film layers with better resistance to oxygen ashing and water absorption. Figure 6 shows the results of post oxygen ashing extinction coefficient reduction as a function of different processes for three different extinction coefficient films. Similarly, figure 7 shows the extinction coefficient change after nine day shelf life monitoring. The processes include single high frequency with argon, single high frequency with helium, mixed high and low frequency with argon, mixed high and low frequency with helium and mixed high and low frequency with slow deposition rate. High frequency is 13.56 MHz and low frequency is less than 1 MHz. Mixed frequency plasma is exposure to both frequencies.

[00100] Figure 8 shows the results of compressive stress testing as a function of the different processes for three different extinction coefficient films. These results illustrate how using helium as a carrier gas results in higher compressive stress values. The mixed high and low frequency plasma had higher compressive stress results. The lowest extinction coefficient films have higher compressive stress results than the higher extinction coefficient films.

[00101] Chart 3 summarizes the results of the cross-sectional SEM (XSEM) on 193 nm PR on dielectric antireflective coating.

Recipe	Stress MPa	FTIR		Lithography Top Down scums/footing
		Si-OH at 3650 7 days in air	cm -1 85/85	
SION		No	No	
SF AR LK	-50	Yes	Yes	not good
SF HE LK	-104	Yes	Yes	not good
MF AR LK	-156	No	No	not good
MF HE LK	-162	No	No	good
MFHE Slow	-258	No	No	good
SF AR MK	-43	Little	Little	not good
SF HE MK	-89	Little	Little	not good
MF AR MK	-125	No	No	not good
MF HE MK	-154	No	No	not good
SF AR HK	-26	Very Little	Very Little	not good
SF HE HK	-59	Very Little	Very Little	not good
MF AR HK	-81	No	No	good
MF HE HK	-132	No	No	good

[00102] Chart 3. Summary of film property stress, FTIR, and lithography test results.

[00103] Another way to make nitrogen free dielectric anti-reflective coating free of basic radicals is to coat the antireflective coating. Scanning electron microscope testing of an amorphous silicon treated antireflective coating revealed no observable footing.

[00104] While the foregoing is directed to preferred embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.